MULTI-SAMPLE READ CIRCUIT HAVING TEST MODE OF OPERATION

BACKGROUND

[0001] Multi-sample read operations can be performed in certain non-volatile memory devices. Consider the example of a resistive cross point array of non-volatile memory cells. A multi-sample read operation may be performed on a selected memory cell in the array by taking a first sample of the memory cell, and then taking one or more subsequent samples. The first sample generates a value corresponding to the logic value stored in the selected memory cell. The subsequent samples are used to generate a reference value. A comparison of the first-sampled value and the reference value indicates whether the first-sampled value corresponds to a logic '1' or a logic '0.'

[0002] This multi-sample read operation is considered self-referencing because the first-sampled value is not compared to an external reference. Self-referencing read operations in general tend to be more reliable than read operations in which sensed values are compared to an external reference values. Moreover, due to limitations on the fabrication of certain cross point memory cell arrays, it can be difficult to find a single reference value for all of the memory cells in a large array.

[0003] Digital sense amplifiers can be used to perform multi-sample read operations on non-volatile memory. Consider the example of a digital sense amplifier including an integrator and a digital counter. A sense operation involves integrating a charge at a rate that depends upon the logic state of the selected memory cell, and determining the time for the charge to reach a threshold (the first sample may include one or more sense operations). The time is determined by using the digital counter to count clock pulses. A reference count is then subtracted from the clock pulse count (in a self-referencing operation, one or more samples are taken to generate the reference count). If $CNT_0 < CNT_R < CNT_1$, the most significant bit of the count indicates whether the logic value initially stored in the selected memory cell was a

logic '1' or a logic '0' (CNT_R is the reference count, CNT_0 is the count corresponding to a logic 0, and CNT_1 is the count corresponding to a logic 1).

[0004] Certain digital sense amplifiers output only the most significant bit of the count. The full contents of the digital counter are not made available.

[0005] During testing of the resistive cross point array, however, it can be helpful to know the contents of the digital counters, not just the sign of the most significant bit. The count at the end of the read operation can be used to determine signal-to-noise ratio (SNR). Measured as the ratio of the signal out of the digital amplifier to the noise generated within the digital amplifier where the signal is taken out, the SNR is a measure of reliability.

[0006] It would be desirable have the ability to determine the contents of the digital counter at the end of a multi-sample read operation. It would also be desirable to add this ability with a minimal amount of circuitry, since adding circuitry can increase the cost of the memory.

SUMMARY

[0007] According to one aspect of the present invention, a data storage device includes non-volatile memory; and a read circuit for performing multi-sample read operations on the memory during a normal mode of operation. The read circuit includes a digital counter having an output that indicates a single bit. The read circuit allows test clock pulses to be applied to the digital counter during a test mode. The test clock pulses can be counted to determine a state of the digital counter.

[0008] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is an illustration of a read circuit for performing read operations on non-volatile memory in accordance with an embodiment of the present invention.

[0010] Figure 2 is an illustration of a method of operating a read circuit in a normal mode in accordance with an embodiment of the present invention.

[0011] Figures 3a-3c are illustrations of methods of operating a read circuit in test modes in accordance with different embodiments of the present invention.

[0012] Figure 4 is an illustration of a data storage device in accordance with an embodiment of the present invention.

[0013] Figure 5 is an illustration of a memory tester in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0014] As shown in the drawings for purposes of illustration, the present invention is embodied in a read circuit including a digital sense amplifier for performing multi-sample read operations on non-volatile memory. The non-volatile memory is not limited to any particular type. Although examples involving Magnetic Random Access Memory ("MRAM") will be used below, the read circuit is not limited to MRAM. The read circuit can be used with other types of resistive cross point random access memory arrays, including but not limited to arrays of phase change memory, polymer memory, and molecular memory. The read circuit can also be used with forms of resistive cross point anti-fuse write once memory.

[0015] The digital sense amplifier is not limited to any particular type. See, for example, assignee's U.S. Patent No. 6,188,615, which is incorporated herein by reference.

[0016] Reference is made to Figure 1, which illustrates a read circuit 110 coupled to a non-volatile memory device 112. The read circuit 110 may be connected directly to the memory device 112, or it may be coupled indirectly to the

memory device 112. The read circuit 110 may be indirectly coupled to the memory device 112 if, for example, the memory device 112 is part of a large memory cell array.

[0017] The read circuit 110 includes a digital sense amplifier 114, a control gate 116, a sample/hold (S/H) 118, and a digital counter 120. Asserting a reset signal sets the state of the digital counter 120 to zero. Asserting a preset signal loads the state of the S/H 118 into the digital counter 120. Asserting a S/H signal loads the state of the digital counter 120 into the S/H 118. Asserting an invert signal causes the S/H 118 to change the sign of its state. Sequencing logic 122 can assert these signals at the appropriate times.

[0018] The read circuit 110 is operable in normal and test modes. During the normal mode of operation, the control gate 116 connects an output of the digital sense amplifier 114 to an input of the digital counter 120. During the test mode of operation, the control gate 116 disconnects the output of the digital sense amplifier 114 and instead allows an external source (not shown) to supply test clock pulses (CLK_T) to the input of the digital counter 120.

[0019] The control gate 116 is not limited to any particular implementation. However, a simple implementation is illustrated in Figure 1. The control gate 116 of Figure 1 includes a NOR gate 116a and a NAND gate 116b. A first input of the NOR gate 116a is adapted to receive a signal (MOD) indicating the mode of operation. A second input of the NOR gate 116a is connected to an output of the digital sense amplifier 114. A first input of the NAND gate 116b is connected to an output of the NOR gate 116a. A second input of the NOR gate 116a is adapted to receive the test clock pulses (CLK_T) from the external source. An output of the NAND gate 116b is connected to an input of the digital counter 120.

[0020] A multi-sample read operation is performed when the normal mode of operation is commanded (via the signal MOD). The multi-sample read operation may be performed as follows. A first sample of the memory device 112 is taken. The digital sense amplifier 114 senses the state of the memory device 112, and provides a stream of clock pulses (CLK_S), the number of which represents the state of the memory device 112. The control gate 116 routes the sense clock pulses (CLK_S) to

an input of the digital counter 120. The digital counter 120 counts the number of clock pulses (CLK_S). At the end of the sense operation, the count stored in the digital counter 120 represents the logic value stored in the memory device 112.

[0021] Additional sense operations may be performed during the first sample. The digital counter keeps a running sum of the results of these sense operations.

[0022] At least one additional sample is then taken to establish a reference count. Each additional sample may involve writing a known value to the memory device 112 and sensing the corresponding state of the memory device 112. The digital sense amplifier 114 generates a stream of sense clock pulses (CLK_S), which the control gate 116 routes to the input of digital counter 120.

[0023] During these additional samples, the sense clock pulses (CLK_S) reduce the count in the digital counter 120. In this manner, the reference count is subtracted from the count representing the stored logic value.

[0024] At the end of multi-sample read operation, the sign-bit of the digital counter 120 is examined. The sign-bit indicates whether a logic '1' or a logic '0' was sensed during the first sample.

[0025] In the alternative, the digital sense amplifier 114 may take a first sample, and save the count, then take at least one additional sample to establish a reference count, and then compare the stored count to the reference count. An output of the comparison is equivalent to the sign-bit of the digital counter 120.

[0026] The multi-sample read operation is destructive since the logic value sensed during the first sample was overwritten. Therefore, the logic value is written back to the memory device 112 at the end of the read operation. An exemplary three-sample read operation is illustrated in Figure 2 and described below

[0027] At the end of the multi-sample read operation, the read circuit 110 outputs the sign-bit of the count, but not the full count in the digital counter 120. However, when operated in the test mode, the read circuit 110 allows the full count to be determined.

[0028] Reference is made to Figure 2, which describes a three-sample read operation. The read circuit 110 is not limited to a three-sample read operation

Two samples could be taken, or four or more samples could be taken. The three sample read operation is provided merely as an example.

[0029] The reset signal is asserted, whereby the counter 120 is reset to zero (210). A first sample of the memory device 112 is taken by performing two consecutive sense operations on the memory device 112 (220). During the first sense operation, the digital sense amplifier 114 sends sense clock pulses (CLK_S) to the digital counter 120. The number of sense clock pulses (CLK_S) represents the logic value stored in the memory device 112. During the second sense operation, the digital sense amplifier 114 once again sends sense clock pulses to the digital counter 120. The additional number of pulses represents the logic value stored in the memory device 112. The count in the digital counter 120 is cumulative, in that it is not reset after each sense operation. Thus far, the count in the digital counter 120 indicates the number of pulses occurring during both the first and second sense operations.

[0030] The contents of the digital counter 120 are shifted to the S/H 118, and then the S/H 118 shifts the negative value back to the digital counter 120. Hence the sign-bit of the digital counter 120 is flipped to negative (230).

[0031] A second sample is taken (240). A first logic value is written to the memory device 112, and a sense operation is performed. The number of sense clock pulses (CLK_S) that occur during the second sample represents the first logic value. Each of these sense clock pulses (CLK_S) causes the digital counter 120 to count up (the negative count becomes less negative). At the end of the second sample, the count is increased by the number of pulses that represent the first logic value.

[0032] A third sample is taken (250). A second logic value is written to the memory device 112, and a sense operation is performed. The number of sense clock pulses (CLK_S) that occur during the third sample represents the second logic value. Each of these sense clock pulses (CLK_S) causes the digital counter 120 to count up. At the end of the third sample, the value in the digital counter is $-CNT_{read1} - CNT_{read2} + CNT_{logic1} + CNT_{logic2}$.

[0033] The most significant bit of the count indicates the logic value that was sensed during the first sample.

[0034] Consider the example of a magnetic tunnel junction. The magnetic tunnel junction has an initial resistance of R, which corresponds to a first logic value. The count representing this logic value is (ideally) X. The resistance R(1+TMR) corresponds to second logic value, and is represented by the count X+Y, where Y>0, and TMR is the tunneling magnetoresistance ratio of the magnetic tunnel junction. Table 1 summarizes the state of the digital counter 120 at various points in the triple-sample read operation. At the end of the third sample, the state of the digital counter 120 has a positive sign (since Y>0). This indicates that the first logic value was initially stored in the memory device 112. Had the second logic value been initially stored in the memory device 112, the digital counter state at the end of the third sample would have been –Y, and the sign-bit would have been negative.

TABLE 1

Operation	Counter state
Sense 1, sample 1	X
Sense 2, sample 1	2X
Change sign	-2X
Sense, sample 2	-X
Sense, sample 3	Y

[0035] This multi-sample read operation is destructive, since the initial logic value is overwritten. Therefore, the initial logic value is restored (260), if the initial logic value is different than the logic value written during the third sample.

[0036] Different test modes can be selected. The different test modes determine the digital count at different stages of a multi-sample read operation.

[0037] During the test mode, the contents of the digital counter 120 are shifted to the S/H 118, and then the S/H 118 shifts the negative value back to the digital counter 120. The external source supplies test clock pulses (CLK_T) to the input of the digital counter 120, which causes the digital counter 120 to count up. The test

clock pulses (CLK_T) are supplied until the sign-bit indicates that the sign changes (that is, the count is zero). The test clock pulses (CLK_T) are counted until the sign-bit changes. The count of test clock pulses (CLK_T) is equal to the count that was shifted to the S/H 118 at the beginning of the test mode. The original count can be restored to the digital counter 120 by shifting the contents of the S/H 118 back into the digital counter 120.

[0038] Reference is now made to Figure 3a, which describes an exemplary test mode A. Test mode A is commanded after a multi-sample read operation has been performed. The objective of test mode A is to determine the state of the digital counter 120 at the end of the read operation.

[0039] An external source supplies a total of NT test clock pulses (CLK_T) to the input of the digital counter 120 (310), whereby the count CNT is increased by NT. CNT is the count in the digital counter 120 at the end of the multi-sample read operation, and NT is a number of counts that is assumed to be larger than the most negative count that may be sensed. When NT is added to the contents of the digital counter 120, the resulting count will always be positive (i.e., the MSB will always be 0).

[0040] The count CNT+NT is copied to the S/H 118 (312). The digital counter is then preset with the negative of the state stored in the S/H 118 (314).

[0041] The external source supplies and counts test pulses to the input of the digital counter 120 until the sign-bit indicates that the sign of the digital counter state has changed (316). This additional number of pulses is designated as ΔnT.

[0042] The amount of margin is computed (318). The amount of margin may be computed as m=NT-CNT if $\Delta nT < NT$, and n=CNT-NT CNT if $\Delta nT > NT$. The interpretation of 'm' is the margin of a sign-bit that is '0' MSB, and 'n' is the margin of a sign-bit that is '1'.

[0043] These margins represent the signal out of the digital sense amplifier 114. The larger the margins, the larger the sense signal that had been generated by the multi- sample read operation. Noise can be measured for the multi-sample read operation by performing the sense operation without writing the reference bits. An ideal margin value for the output from the noise sensing would be 'm' or 'n' equal to 1

or 0. A noise characterization of the digital sense amplifier 116 may represent hundreds or thousands of noise sense operations and the values for 'n_noise' and 'm_noise' may be greater than '1' or '0' due to various noise sources affecting the sense counts during the sense operations. The SNR for the digital sense amplifier 114 may be defined as the ratio of the sense margin 'm' divided by the noise sense margin 'm_noise' to define the SNR for a MSB of '0' and as the ratio of the sense margin 'n' divided by the noise sense margin 'n_noise' to define the SNR for a MSB of '1'.

[0044] Reference is now made to Figure 3b, which describes an exemplary test mode B. Test mode B is commanded after a multi-sample read operation has been performed. The objective of test mode B is also to determine the value of the digital counter 120 at the end of the multi-sample read operation.

[0045] The sign-bit is examined (350). If the sign-bit indicates a negative value, the external source supplies test clock pulses (CLK_T) to the digital counter 120, until the digital counter 120 counts up to zero (352). The external source supplies and counts the test clock pulses (CLK_T) until the sign-bit indicates that the digital counter state has reached zero.

[0046] If the sign-bit is '0', the digital counter state is transferred to the S/H 118, and the digital counter 120 is preset to the negative of the value in the S/H 118 (354). The external source supplies test clock pulses (CLK_T) to the digital counter 120, until the sign-bit flips to zero (352). The test pulses are counted until the sign-bit changes (356).

[0047] Reference is now made to Figure 3c, which describes a test mode C. The objective of test mode C is to determine the state of the digital counter 120 sometime during the multi-sample read operation. Thus test mode C is commanded sometime during the multi-sample read operation.

[0048] The state of the digital counter 120 is shifted to the S/H 118 (370), and the digital counter 120 is preset with the negative of the state of the S/H 118 (372). The external source supplies and counts test clock pulses (CLK_T) to the digital counter 120 until the sign-bit changes (374). The counted number of test clock pulses (CLK_T) is equal to the state of the digital counter 120 when test mode C was

commanded. The digital counter 120 is preset to the value in the S/H 118 (thereby restoring the state of the digital counter 120), and the multi-sample read operation is resumed.

[0049] Reference is made to Figure 4, which illustrates a data storage device 410 including a resistive cross point array 412 of memory cells 414. Bit lines 416 extend along columns of the array 412. One read circuit 110 is provided for multiple columns. During a read operation, a multiplexer 418 connects a read circuit 110 to a selected bit line 416. The outputs (sign-bits) of the read circuits 110 may be connected in a scan chain, which terminates in a first pin 420. The inputs to the read circuits 110 (for the test clock pulses) may be connected in a scan chain, which terminates in a second pin 422.

[0050] Reference is now made to Figure 5. A memory tester 510 includes a clock generator 512 for providing the test clock pulses to the read circuit 120. The tester 510 can also include a circuit 514 for examining the sign-bit, and a counter 516 for counting the number of test clock pulses until the sign-bit changes. The state of the counter 516 can be displayed by the memory tester 510.

[0051] The memory tester 510 may be separate from the data storage device 410. The memory tester 510 can be connect to the first and second pins 420 and 422. The first pin 420 provides the sign-bit to the tester 510. The memory tester 510 provides the test clock pulses to the second pin 422.

[0052] The memory tester 510 may also include a module 518 for determining the relative performance of the data storage device 410. For example, the memory tester 510 may perform a binning function on a plurality of different data storage devices. Binning is a process of sorting chips according to some performance parameter. For example, the data storage devices could be binned by separating them according to the value of the first sense count performed during the first sample. The faster data storage devices would come from the bin with the smallest sense counts. As another example, the data storage devices could be binned on SNR, which roughly specifies the expected reliability of the sense operations.

[0053] The present invention is not limited to the specific embodiments described above. Instead, the present invention is construed according to the claims the follow.